

REMARKS

I. Introduction

In response to the pending Office Action, Applicants have amended claim 11 to further clarify the intended subject matter of the invention. No new matter has been added.

Applicants note with appreciation the indication of allowable subject matter recited in claims 14 and 15 of the pending application.

For the reasons set forth below, Applicants respectfully submit that all pending claims are patentable over the cited prior art.

II. The Rejection Of Claims 11-13 And 16 Under 35 U.S.C. § 103

Claims 11-13 and 16 were rejected under 35 U.S.C. § 103(a), as being unpatentable over Jarwala et al. (USP No. 5,673,276) in view of Komoike (USP No. 6,094,736) and Yamamura (USP No. 5,341,096). Applicants respectfully traverse these rejections for at least the following reasons.

Claim 11, as amended, recites, in part, a semiconductor device comprising...an internal scan chain for an internal scan test provided in each of said chip IPs, wherein the boundary scan test circuit and the internal scan chain for an internal scan test are formed so as to be capable of performing an internal scan test simultaneously with each other for testing said test object (DUT), using test data for an internal scan test which is input from outside, and the boundary scan test circuit performs a boundary scan test in a boundary scan test mode and an internal scan test in an internal scan test mode.

One feature of the present invention is the boundary scan test circuit performs an internal scan test when an internal scan test using test data input from the outside is performed, in addition to performing a boundary scan test in a boundary scan test mode. One result of this feature is that the time needed perform internal tests is shortened and a high detection rate is achieved.

It is alleged that Jarwala teaches that the boundary scan test circuit and the internal scan chain for an internal scan test are formed so as to be capable of performing a boundary scan test and an internal scan test simultaneously with each other for testing the combinatorial circuit using test data for an internal scan test which is input from outside. However, Jarwala fails to disclose the amended feature that the boundary scan test circuit performs a boundary scan test in a boundary scan test mode and an internal scan test in an internal scan test mode. Nor are Komioke and Yamamura relied upon to remedy this deficiency.

Moreover, none of the devices disclosed in the cited prior art references exhibit the desired feature of detecting failures with a superior detection rate by making the boundary scan test circuit also perform an internal scan test when an internal scan test using test data input from outside is performed.

In order to establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 180 USPQ 580 (CCPA1974). As Jarwala, Komoike and Yamamura, at a minimum, fail to teach or suggest a semiconductor device wherein the boundary scan test circuit performs a boundary scan test in a boundary scan test mode and an internal scan test in an internal scan test mode, it is submitted that Jarwala, Komoike and Yamamura, alone or in combination do not render claim 11 obvious.

Accordingly, it is respectfully requested that the § 103 rejection of claim 11, and any pending claims dependent thereon be withdrawn.

III. All Dependent Claims Are Allowable Because The Independent Claim From Which They Depend Is Allowable

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claim 11 is patentable for the reasons set forth above, it is respectfully submitted that all pending dependent claims are also in condition for allowance.

IV. Conclusion

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication of which is respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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